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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/669,590	09/23/2003	Walter Snoeijs	36145	7859

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EXAMINER	
YOUNG, BRIAN K	

ART UNIT	PAPER NUMBER
2819	

DATE MAILED: 02/22/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/669,590	SNOEIJS, WALTER	
	Examiner	Art Unit	
	Brian Young	2819	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 November 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-55 and 58-65* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *1-54 and 61-65* is/are allowed.

6)☒ Claim(s) *55* is/are rejected.

7)☒ Claim(s) *58-60* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *23 September 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claim 55 is rejected under 35 U.S.C. 102(b) as being anticipated by Hariharan et al.

Hariharan et al disclose in the FIG. 1 embodiment, a Q.sub.2 pulse closes switches 22, 34 and a sample "n" of the input waveform at terminal 20 is taken across capacitor 26 where it is held. Claim 55 recites "a current sample-and-hold or track-and-hold circuit, wherein an input current is injected into a terminal of a component or circuit to convert the input current to a voltage so that this voltage can be stored on a storage capacitor, and where the input current is transferred to another terminal of this component or circuit from where it is made available for further use". Hariharan et al disclose (1/3)T later a Q.sub.3 pulse closes switch 52 setting amplifier output 44 to zero. (1/3)T later a pulse Q.sub.l closes switches 28, 36 and the sampled-and- held on capacitor 26 for (W3)T appears at output 44 of amplifier 40 and is held on capacitor 46 until (1/3)T later when the next Q.sub.2 pulse closes switch 54 and the sample "n" appears at output 62 of sample and hold amplifier 64 and at the same time closes switches 22, 34 where a sample "n+1" of the input wave form at terminal 20 is taken. Sample "n" is time delayed by a period T between terminals 20 and 64. Sample "n+1" and 1 succeeding samples, are likewise time delayed by a period T.

Newly amended claim 55 further recites "wherein the component is a transistor or transconductor or the circuit **includes** a transistor or transconductor." It is clear the from figure 1 of Hariharan et al that their circuit **includes** transistors (22,28,52,34,36,54). The previous language of the newly incorporated claims did not recite "includes". See below:

56. (original) The current sample-and-hold or track-and-hold circuit of claim 55, where said component or circuit is a transistor.

57. (original) The current sample-and-hold or track-and-hold circuit of claim 56, where said component or circuit is a transconductor.

3. Claims 1-54 and 61-65 are allowed.

4. Claims 58-60 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

5. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Fujimoto discloses a sample-and-hold amplifier circuit has a switch, provided between an operational amplifier stage and an inverting amplifier stage, for connecting or cutting off the connection of the operational amplifier stage and the inverting amplifier stage. During the first operation phase (.phi.1), the first and second switches are switched to the .phi.1 side, the third switch is conductive, and the switch for connecting or cutting off the connection is nonconductive. Thus, sampling can be carried out so that first and second capacitors are charged by predetermined electrical charges. During the second operation phase (.phi.2), the first and second switches are switched to the .phi.2 side, the third switch is nonconductive, and the switch for connecting or cutting off the connection is conductive.

Hasegawa discloses A sub-A/D converter of a first stage is constituted by a serial-parallel A/D converter, which does not use a subtractor, comprising two sub-A/D converters and a first D/A converter. A subtracting amplifier includes a subtractor selecting an analog input signal or the output of the first D/A converter and subtracting the output of a second D/A converter from the selected signal, and an amplifier amplifying the output of the subtractor. The subtracting amplifier is provided for each of a plurality of comparators, which are capable of receiving inputs in timeshared fashion, constituting a sub-A/D converter of a second stage.

Nayebi discloses A track and hold apparatus having a track mode and a hold mode, said track and hold apparatus comprising:

an input stage having an input terminal for receiving an input signal;

an output stage having an input terminal and an output terminal;

a holding capacitor coupled to said input terminal of said output stage;

an NMOS transistor coupled between said output terminal of said input stage and said input terminal of said output stage, said NMOS transistor turned on during said track mode and turned off during said hold mode;

a PMOS transistor coupled between said output terminal of said input stage and ground, said PMOS transistor turned on during said hold mode and turned off during said track mode; and a switch driver for turning said NMOS and PMOS transistors on and off, said switch driver generating a single clock signal received by both said NMOS and PMOS transistors, said single clock signal turning said NMOS transistor off before turning said PMOS transistor on during transition from said track mode to said hold mode.

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Brian Young whose telephone number is 571-272-1816. The examiner can normally be reached on Mon-Fri 7:30-4:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mike Tokar can be reached on 571-272-1812. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Brian Young
Primary Examiner
Art Unit 2819

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